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by

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for

METHOD OF FABRICATING BOTTLE TRENCH CAPACITORS USING AN ELECTROCHEMICAL ETCH WITH ELECTROCHEMICAL ETCH STOP

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates generally to semiconductor devices. More particularly, the present invention relates to methods of making and the structure of trench capacitors in memory devices.

Background Information

[0002] The semiconductor industry requires miniaturization of individual devices such as transistors and capacitors to accommodate the increasing density of circuits necessary for semiconductor products. One common semiconductor product is a dynamic random access memory ("DRAM"), which may incorporate billions of individual DRAM memory units (cells), each capable of storing one data bit. A DRAM cell includes a planar access transistor and a storage capacitor. The access transistor transfers charge to and from the storage capacitor to read or write data. The total amount of charge stored in the capacitor must exceed a threshold value, which is based on the minimum amount of charge required to read the capacitor by a sensing device, and the frequency at which the capacitors are re-charged (refreshed). Because the capacitors do not retain their charge for an infinite time, periodic capacitor refreshing is required to replace leaking charge before the total charge retained falls below the value needed to read a memory cell.

[0003] In order to increase the memory capacity on a chip, i.e., the number of cells, there is a need to shrink the amount of horizontal area on the chip used by each cell,

which requires a reduction in transistor and/or capacitor size. However, as the total cell size is reduced, the amount of charge retained in a horizontal planar capacitor may not be sufficient to ensure proper device operation, since the capacitance is directly proportional to the planar area of the device. One technique to address this problem is to fabricate trench capacitors, which have a trench shape when viewed in cross section and are formed by vertical etching into the silicon substrate, typically using gaseous species. Figure 1a shows an the ideal trench capacitor **1**, where insulator **8** has a U-shape and is bounded on the outside by an outer capacitor electrode (plate) **2**, and on the inside by an inner plate **7**. Plate **2** represents the 'bottom' plate formed by doping the silicon substrate and contains surfaces **3**, **3'**, and **4**, with dimensions, d1, d2, and w1, respectively. In a cylindrical trench, surfaces **3** and **3'** are part of the same cylinder wall. Similarly, the "top" plate **7** has vertical surfaces **6**, **6'**, and horizontal surface **5**, which are approximately the same dimensions as bottom plate surfaces, **3**, **3'**, and **4**, respectively.

[0004] In terms of behavior and size, it is well known to those skilled in the art that the ideal trench capacitor of Figure 1a can be approximated by an equivalent planar capacitor shown in Figure 1b, containing plates **11**, **13** and insulator **12**, whose width W equals the sum of d1, d2, and w1. In current technology, a trench typically has a depth in the range of 4-8 μm and an oval or rounded top-down-view shape, with a horizontal dimension which may be less than 0.5 μm. Referring to Figures 1a and 1b, and assuming the same insulator thickness, a trench capacitor of 0.5 um width (w1) and 4 um depth (d1) has the approximate capacitance of a planar capacitor of 8.5 um width. That is, the trench capacitor is equivalent to a planar capacitor whose width W

is the sum of the trench capacitor width and two times its depth. Thus, the trench capacitor structure permits a large capacitance per planar unit area of substrate, while at the same time allowing the device cell to occupy a small portion of the cell area.

[0005] For a given DRAM cell size, where the size of the horizontal trench opening is fixed, the capacitance in a trench capacitor can be increased simply by increasing the trench depth. However, it is also well known to those skilled in the art that the vertical etch that is used to form the trench typically results in a tapered trench profile, which produces a smaller surface area and therefore lower capacitance than if the trench formed an ideal cylindrical shape. Figure 2 shows "vertical" walls **21, 21'**, and trench bottom **22**. The walls taper in during etch, causing the bottom of the trench to taper toward a point. The tapering is due in part to the increased ratio of depth to width in the trenches as they are etched deeper, which reduces the ability of the gaseous etching species impinging from outside the trench to strike the outer portions of the trench bottom. Thus, for a given planar hole diameter, there is a limit to the trench depth that is attainable, since the trench walls taper in towards a point.

[0006] Related art teaches methods of forming better trench capacitor geometries, such as the "deep trench bottle etch (BE) process". Figure 3 illustrates the appearance of a trench formed using the BE process. The BE process includes formation of an insulating collar **25**, inside the top of the silicon trench after initial deep trench etch which is used to form surfaces **3, 3'**, and **4**, shown as a dashed line. This is followed by a liquid chemical etch, which removes the silicon residing underneath the collar in the lower part of the trench, and results in a bottle-shaped final profile of the trench. The etch tends to be isotropic; that is, the silicon at the

surface of vertical and horizontal portions of the trench is etched at about the same rate. Figure 3 shows that the final trench contains vertical surfaces **26**, **26'**, and horizontal surface **27**, all larger than their original counterparts **3**, **3'**, and **4**, respectively. In addition, new surfaces **28** and **28'** are formed at the top of the trench, adding to the overall surface area. In this manner, the area of the trench capacitor is made larger by increasing both the depth and the width of the trench.

[0007] It will be appreciated by those skilled in the art that care must be employed to form bottle-shaped trenches using a wet chemical etch in the manner described above. The uniformity of such etches depends on many variables, such as the concentration of active etching species in the liquid etchant, which can vary over time, causing the silicon removal in the lower trench to increase or decrease. Additionally, control of the effective time that the trench is exposed to liquid etchant may be difficult. The etch time employed to form the bottle trench is based on the known etch rate of silicon when subject to a given concentration of etchant. After the desired etch time, wafers containing the DRAM chips are rinsed and dried to dilute, and then remove, the etchant from the bottle trenches and prevent further etching of silicon. However, the extremely small size and bottle shape of the trenches can act to retard liquid etchant removal, resulting in an effective etch time greater than desired. In addition, the etch profile within a trench may not be uniform, due to incomplete or tardy removal of liquid etchant in certain regions such as corners in the trench. For the above reasons, among others, the uniformity of trench size may be difficult to control, and can lead to failures where adjacent bottle trenches merge, as depicted in Fig. 4. Figure 4 illustrates an array of equally-spaced bottle trenches **31**, **32**, **33**, and **34** after

bottle etch and rinse. The profiles are sketched to illustrate less-than ideal final trench shapes that may form for the reasons mentioned above. While the internal surfaces **43** and **44** of trenches **33** and **34**, respectively, remain distinct, surfaces **41** and **42** of trenches **31** and **32**, respectively, have merged leading to a storage failure in the corresponding memory cells.

[0008] A further problem with the bottle etch process described in related art is that the nonunifomity can lead to significantly lower than ideal trench capacitance. In order to reduce the risk of merging of trenches that is inherent in the process, a maximum tolerable trench width can be established, based on the separation distance of adjacent trenches. Then, a nominal bottle etch process recipe is developed to allow for variations in the bottle etch process. Figures 5a-c illustrate examples of three different chemical etch conditions applied to form a bottle trench after an initial vertical etch. Figure 5a shows a group of trenches after chemical etch for the nominal process conditions, which results in trench **51** of width d5. This is the result that obtains when the etch time, etchant concentration, and rinse are all carried out exactly according to the designed etch recipe. The trenches in Figure 5b illustrate the result of trench formation using the minimal tolerable chemical etch condition, which may denote the state where the effective etch time deviates below the nominal time by the greatest allowable amount; and the actual etchant concentration is less than the nominal by the maximum tolerable amount. The resulting trench **52** has width d6, which is less than d5. The converse of Figure 5b is shown in Figure 5c, where the trenches have been etched to the maximum size, width d7, where the effective etch time and concentration exceed the nominal values by the maximum tolerable amount.

The value of d7 minus d6 (V) represents the variability in trench size resulting from the chemical etch process, which may be on the order of tenths of micrometers. The nominal trench size d5, must be smaller than d7 by a value that may be about V/2. Thus, the average capacitor will have a significantly smaller dimension (with concomitantly lower capacitance) than the maximum size capacitor.

[0009] A further result of a large variability in the chemical etch process is the production of many trenches with significantly lower capacitance (or size) than nominal, as illustrated by the capacitor structures shown in Figure 5b.

[0010] In view of the foregoing, it can be appreciated that a substantial need exists for improvement of trench storage capacitors.

SUMMARY OF THE INVENTION

[0011] The present invention relates to structures and processes that improve storage capacitors. In particular, a process is disclosed that overcomes present limitations on production of trench capacitors. An exemplary embodiment of the current invention comprises a bottle trench capacitor structure formed by selective removal of a uniform sacrificial silicon layer of pre-determined thickness from the lower part of the trench. An object of the present invention is to produce bottle trench capacitors in a manner such that the risk of merging adjacent trenches during processing is minimized. This is accomplished in an exemplary embodiment of the current invention by use of a selective chemical etch with a built-in electrochemical etch stop. A bilayer region of silicon in the trench structure is formed such that the surface layer is removed under electrochemical etch without removal of the bottom layer. In this manner the amount of silicon removed from the trenches can be limited, and the problem of merging of adjacent trenches is avoided.

[0012] A further aspect of the present invention relates to the production of trenches of uniform size, such that the capacitance variation between trench devices is minimized. It is well known to those skilled in the art that, in addition to variation in dielectric layer thickness, the primary influence on trench capacitance is the internal trench surface area, which is, in turn, directly proportional to the trench size. In exemplary embodiments of the current invention, the final trench size is in large part determined by removal of a sacrificial silicon layer of well-controlled thickness as detailed below. This results in capacitors of more uniform dimension compared to those produced by conventional processes. An additional object of the current invention is the fabrication of trenches with maximum capacitance attainable for a given DRAM cell size and trench separation. It will be appreciated by those skilled in the art that the more uniform process contained in embodiments of the present invention makes it possible to increase the average trench width without increased risk of failure due to merging of trenches.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figures 1a and 1b represent, respectively, an ideal trench capacitor in cross-section, and its planar capacitor equivalent.

[0014] Figure 2 is a cross section representing realistic trench profiles achieved using standard vertical etch processes.

[0015] Figure 3 is a drawing illustrating a bottle trench formed by a wet chemical etch employed after a standard vertical etch step according to known art.

[0016] Figure 4 is a drawing illustrating bottle trench non-uniformities and failure due to wet chemical etch process variation.

[0017] Figures 5a-c are schematic drawings illustrating the impact of wet chemical etch process non-uniformity on average dimension of bottle trenches.

[0018] Figures 6a-d are drawings illustrating bottle trench formation according to an embodiment of the present invention.

[0019] Figure 7 illustrates details of electrochemical etch processing steps according to an embodiment of the present invention.

[0020] Figure 8 is a drawing illustrating an electrochemical etch apparatus according to another embodiment of the current invention.

[0021] Figure 9 illustrates a current-voltage passivation curve for n-type silicon.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Preferred embodiments of the present invention are described below, with reference made to the enclosed drawings. Before one or more embodiments of the invention are described in detail, one skilled in the art will appreciate that the invention is not limited in its application to the details of trench structure and the arrangement of steps set forth in the following detailed description or illustrated in the drawings. The invention is capable of other embodiments and of being practiced or being carried out in various ways. Also, it is to be understood that the phraseology and terminology used herein is for the purpose of description and should not be regarded as limiting.

[0023] The present invention is related to methods and structures for providing large and uniform DRAM trench capacitors. Current methods of bottle trench capacitor fabrication employ non-selective wet etching of silicon to enlarge the trench below a collar region. This process entails the risk of complete silicon removal between trenches ("trench merge", as shown in Figure 4) if the etch process is not terminated

in a timely fashion. According to an embodiment of the present invention, a selective etch process is employed to form the bottle trench that substantially eliminates the etch variability seen in the related art. Exemplary embodiments are now described in relation to Figures 6-10.

[0024] In Figure 6a, after standard deep trench formation using well known techniques, an insulating collar **60** is fabricated so that it lines the top part of the trench. In an exemplary embodiment, the collar is formed by depositing a photoresist material to line the bottom of the trench, followed by growth of an oxide on the inside surface near the top of the trench. In some embodiments this collar may comprise a nitride, or related material that is resistant to a subsequent bottle etch. After oxide collar formation, the resist in the lower region of the trench is chemically stripped while leaving the oxide collar untouched. In the lower part of the trench the silicon is thus unprotected, forming surface **61**. The adjacent vertical walls of neighboring trenches are separated by distance l_i. After insulating collar formation, an n-type dopant is introduced into the silicon in the lower trench, forming region **62,** as illustrated in Figure 6b. In an exemplary embodiment, this is accomplished by gas-phase doping methods well-known to those skilled in the art. The depth of the n-type doping, t_n, is defined (with reference to Figure 6b) by the vertical distance between the bottom of the trench and the bottom of the n-doped silicon layer, border **63.** This depth extends equally from all trench surfaces, and is preferably large enough so that the n-doped silicon region extends entirely between adjacent trenches, as depicted in Figure 6b. In a preferred embodiment, the doping level is about 1-5E18 cm^{-3}. Subsequently, as illustrated in Figure 6c, a p-type dopant is introduced to the trench

region, extending to a depth t_p, less than that of the n-type region. The concentration of p-type dopant exceeds that of the n-type dopant previously introduced, resulting in a distinct p-type silicon layer **64** extending from the trench surface to a boundary **65** with the n-type layer, as shown in Figure 6c. After p-type layer formation, the dual-doped trench structure contains regions **62** and **64** which are comprised of activated dopants creating a p-n junction at interface **65**. Although not essential to the current invention, it will be appreciated by skilled artisans that the horizontal width of the p-type layer may be substantially equivalent to the vertical depth, t_p, as defined above. Figure 6c further shows that, in an exemplary embodiment, a region of n-type silicon **66** remains between the vertical portion of p-type layers in adjacent trenches. Thus, in an exemplary embodiment of the current invention, t_p is typically less than half of L_i , the spacing between the vertical edges of neighboring trenches. In a preferred embodiment, the level of p-type doping is in the range of $1E19cm^{-3}$ or higher, rendering the layer a "p+" silicon region. It is also to be appreciated that the gas phase doping process allows the growth of layers of highly uniform thickness when compared to the trench dimensions. That is, while overall trench width may be in the range of 100-1000 nm, the expected variation in t_p may be only several nm.

[0025] Subsequently, the trenches are subjected to an electrochemical etch under applied bias voltage, wherein, in a preferred embodiment, the etch solution comprises aqueous solutions comprising water (H_2O) and hydroxide (NH_4OH or KOH). This results in the complete removal of layer **64** while leaving the region **62** substantially intact, forming an exposed n-type silicon surface **67,** as illustrated in Figure 6d. The three dimensional shape of the bottle trench shown in Figure 6d is in part determined

by the shape of the neck region, which is, in turn, determined by the shape of mask used to form the initial vertical trench. Embodiments of the present invention include trenches formed from bottle shaped structures whose neck region in top-down view appears alternatively as an oval, a circle, a square, or a rectangle.

[0026] Figure 7 illustrates an exemplary process flow of an embodiment of the current invention. After processing to form the dual-doped trench structures as depicted in Figure 6c, shown as step **70** in Figure 7, the silicon wafers containing the trench devices are placed in an electrochemical etching apparatus containing an hydroxide/water etch solution, step **71**. In a preferred embodiment, they are placed in a holder within the apparatus, which provides electrical contact to the backside of the silicon wafer, as depicted in Figure 8. A wafer **80** is held by clamps **82**, while an electrical contact is made to the backside wafer surface **81**. An electrical conductor **84** connects to a counter electrode **86**. A bias of approximately +1.2 V is subsequently applied between the wafer backside **81** and the counter electrode **86** in the etching apparatus. Etch step **71** is performed until the p+ silicon layer in the trench is completely removed. The wafer remains in the apparatus and subject to continued applied bias for a subsequent "overetch," step **72**. The overetch step is performed to assure that the p+ layer is removed in all trenches so the overetch time employed preferably accounts for variations in process temperature, etch concentration, and related factors. In a preferred embodiment, the ratio of etch rates of p-type:n-type silicon (p:n etch selectivity) can be as high as 200:1, depending on the exact concentration of hydroxide and the solution temperature. For purposes of example, given nominal etch conditions having a p:n etch selectivity of 100:1 and a

p-type removal rate of a 50 nm layer in 100 seconds, step **71** may be performed for 100 seconds to remove a 50 nm p+ region. Then overetch step **72** to remove any remnant p+ may be performed for an additional 50 second etch time, without substantial risk of etching significantly into the n-silicon region. Under nominal conditions where the 50 nm p-type layer is actually removed in exactly 100 seconds, the 50 seconds overetch of step **72** would remove only 0.25 nm of the n-type silicon region, about one layer of silicon atoms.

[0027] Figure 9 helps explain the mechanism contributing to the enhanced p:n etch selectivity employed in the current invention. The graph shows that above a certain potential Si passivates (> -0.8 V). This characteristic applies for both n-type and p-type silicon. However, since the trench structure contains a reverse biased n/p junction, no current flows through the junction. Thus, the potential drop occurs at the n/p junction and not at the surface of the p layer where it contacts the etch solution. Thus, this leaves the p surface unbiased at open circuit potential and the p-type silicon is subject to continual hydroxide etch. When the n-type silicon is exposed, the current rises and causes immediate passivation of the surface, blocking any further etching.

[0028] After electrochemical etch to remove the sacrificial p-type layer, conventional steps, well-known to skilled artisans, are employed, including silicon doping to form the buried plate of the capacitor, step **73** in figure 7, followed by capacitor dielectric deposition **74** and trench top electrode formation **75**.

[0029] An advantage of the current invention is that because of the high selectivity of the electrochemical etch step, the n-type layer **62** shown in Figure 6b acts as an etch

stop, where the etch rate approaches zero once the n-silicon layer is contacted. Thus, the wet etch process no longer needs to be precisely controlled to determine the amount of silicon removed. Because the etch rate of n+ silicon is so low, one can vary etch concentration, time, and temperature within a wide range, without substantially altering the amount of silicon removed. Thus, in a preferred embodiment of the present invention, the amount of silicon removed during chemical etch is no longer determined by variations in the wet chemical etch process. Rather, the total silicon removed is simply determined by the depth of layer **64,** t_p, since the etch process essentially terminates when the n-type layer **62** is encountered. Thus, as long as t_p is sufficiently small that etch stop layer **66** remains between adjacent trenches, the chance of trench merge can be virtually eliminated.

[0030] As previously noted, another advantage of the present invention is the ability to fabricate larger bottle trenches for a given DRAM cell size. Referring to Figures 5a-c, it is noted that in the present invention the variation in the amount of trench silicon removed, V, does not significantly depend on etch process variation, since the process is designed to remove all of the p+ layer without removing a significant amount of n-silicon. Thus, V arises only from variation in t_p, which is on the order of a few nm. This affords the possibility of designing the nominal trench width to be much greater than in the conventional process, where no etch stop exists, resulting in a much larger V. A still further advantage of the current invention is that since V is so small, the variability in capacitance of trench capacitors among different DRAM cells is minimized.

[0031] An additional advantage of the current invention is that it is possible to scale the process so that it can be successfully employed in smaller DRAM cells in subsequent technologies. That is, as overall trench spacing decreases to accommodate greater device density and performance, the amount of silicon removed in the electrochemical etch process can be easily reduced. This is because the latter depends solely on the thickness of the sacrificial p-type layer, which is determined by precise doping methods.

[0032] Embodiments of structures and methods for fabrication of deep trench capacitors with enhanced uniformity and resistance to structural failure during processing have been described. In the foregoing description, for purposes of explanation, numerous specific details are set forth to provide a thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the present invention may be practiced without these specific details. Furthermore, one skilled in the art can readily appreciate that the specific sequences in which methods are presented and performed are illustrative and it is contemplated that the sequences can be varied and still remain within the spirit and scope of the present invention.

[0033] In the foregoing detailed description, structures and methods in accordance with embodiments of the present invention have been described with reference to specific exemplary embodiments. Accordingly, the present specification and figures are to be regarded as illustrative rather than restrictive. The scope of the invention is to be defined by the claims appended hereto, and by their equivalents.